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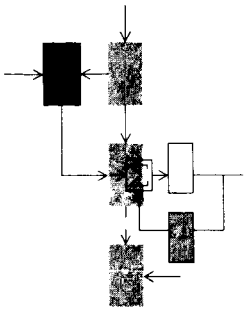

PART 1
COMPUTER-AIDED ELECTRONIC CIRCUIT DESIGN

PART 11
CONDUCTION PROCESSES IN THIN FILMS

Status Report

December 1, 1964 - May 31, 1965

Electronic Systems Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY, CAMBRIDGE 39, MASSACHUSETTS

Department of Electrical Engineering

June, 1965 Status Report ESL-SR-245 Copy No. 49

(PART I)

COMPUTER-AIDED ELECTRONIC CIRCUIT DESIGN

and

(PART II)

CONDUCTION PROCESSES IN THIN FILMS

Status Report

December 1, 1964 - May 31, 1965

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ABSTRACT

Reported upon in Part I is a computer program which makes it possible to analyze electrical networks consisting of linear and nonlinear resistors, inductors, and capacitors excited by voltage and current sources which may be arbitrary functions of time. Circuit configurations and analytical results are displayed on a cathode-ray-tube output of a time-shared computer. Also presented is a summary of work under way in logic design and synthesis through use of a digital computer. A low-cost teletype-operated graphical display is described as well as a new approach to nonlinear circuit analysis through use of a computer.

Part II relates to conduction processes in thin films. This work is motivated by a desire to understand better mechanisms by which conduction takes place in thin semi-insulating films and between sandwich layers of these films. Cadmium sulfide is used as a vehicle for the investigations. Topics reported upon include: thermally stimulated emission currents in CdS; measurements of barrier height, barrier width, and immobility density; optically modulated conductivity with voltage de-excitation; grid-structure formations of metal films; triode construction and formation of blocking grid contact; fringe-step measurements; negative resistance in CdS films; and P-type CdS films.

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PART I

COMPUTER-AIDED ELECTRONIC CIRCUIT DESIGN

CONTENTS

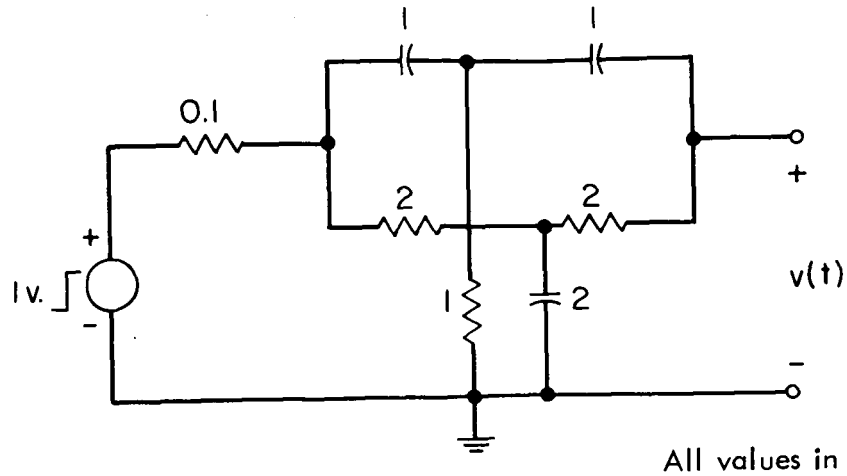
A. DIGITAL COMPUTER SIMULATION OF ELECTRICAL NETWORKS

Professor M. L. Dertouzos
Mr. Charles W. Therrien,
Graduate Student

A method is being investigated for the on-line simulation of electrical networks. This method treats networks consisting of linear and nonlinear resistors as well as inductors and capacitors. A given network can be excited with voltage and current sources which may be arbitrary functions of time. The voltage response across any node in the network may then be called for as output.

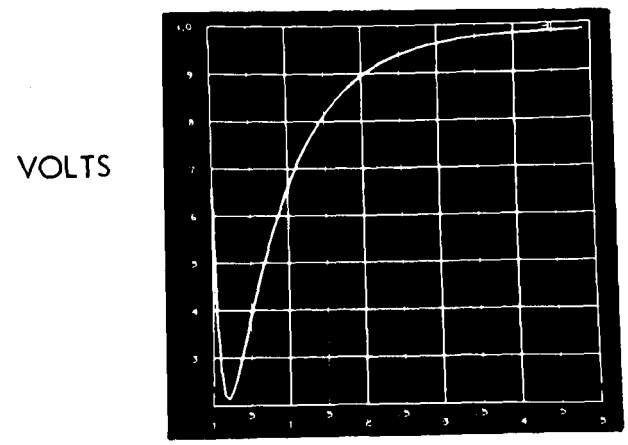
The computer model for the network consists of lists of storage registers representing the branches connected to other lists representing the nodes. The method for solution at each instant of time is as follows: The nodes are assigned fixed node potentials. The voltage across each branch, and hence the current through it, is determined by the two nodes to which it is connected. Equilibrium requires the sum of the branch currents at each node to be zero. If the sum is not zero, new node potentials closer to the equilibrium values are computed by perturbing the old ones in a prescribed manner. This process is repeated until the equilibrium values are obtained within a specified tolerance.

Thus far, a computer program for use on the Project MAC time-sharing system has been written to apply the foregoing method to linear RLC networks excited with step and sinusoidal current and voltage sources. The program computes an accurate solution to any given linear network. Computer time for solution of networks containing up to about 8 nodes and 12 branches is of the order of a few seconds. An example of a circuit analyzed by the foregoing program is shown in the accompanying illustration.



All values in ohms, henrys, and farads

(a) Twin-T Filter



(b) voltage v(t) in Response to Unit Step

Response of a Twin-T Filter as Computed and Plotted by the Circuit-Analysis Program

B. AN INPUT-OUTPUT PROGRAM FOR ELECTRONIC CIRCUITS USING CATHODE RAY TUBE

Professor M. L. Dertouzos
Mr. Arthur A. Dvorak, Jr.,
Undergraduate Student

A computer program has been written which allows an operator to portray quickly and easily planar electronic circuits on the Electronic Systems Laboratory console display at Project MAC. Circuit elements are formed by moving a tracking light pen to the desired position on the screen and actuating an "element button". Circuit characteristics are described in a list structure with pointers. Used in conjunction with the analysis program described above, circuits with multiple elements can be displayed and their response to various types of excitation readily determined.

C. ON-LINE SWITCHING-FUNCTION SYNTHESIS WITH ARBITRARY SETS OF LOGIC GATES

Professor M.L. Dertouzos
Mr. Paul J. Santos, Jr.,
Research Assistant

The central aim of logical design is the synthesis of any given switching function in terms of given sets of elementary building blocks, for the optimization of some performance index in the presence of constraints. Although present state of the art yields algorithmic methods for the solution of certain specific instances of the problem (such as minimization of building-block inputs with a two-level, AND-OR realization), no fully algorithmic method exists for the solution of the more general problem.

Solutions to the general problem are being developed through use of an on-line computer process in which the machine accomplishes those computational tasks which can be algorithmically specified and the user provides those decisions which he is better qualified to make. The machine portion of the system is based on a set of heuristic procedures which subject to certain conditions guarantee convergence of the process. Results obtained to date indicate that this method of synthesis yields more economical structures than those obtained by brute-force alternatives.

using successive local-optimization procedures, and does not depend on impractical (and usually impossible) exhaustive searches through all possible solutions. It is expected that a report on this work will be issued during the Fall, 1965.

D. SINGLE THRESHOLD ELEMENT REALIZABILITY BY MINIMIZATION

Professor M.L. Dertouzos
Mr. Zachary Fluhr,
Graduate Student

Previous work[1] has shown that the problem of determining whether an arbitrary Boolean function of N variables is realizable with a single threshold element can be reduced to the problem of minimizing a quantity which is a function of N+1 variables. Several properties of this quantity are being derived and studied. It can be shown, for example, that the quantity may be interpreted geometrically as a structure of intersecting N+1 dimensional hyperplanes. Each of these hyperplanes corresponds to some N-variable Boolean function, and if the given Boolean function is realizable, its associated hyperplane will be "flat" with zero height. The hyperplanes are so situated that they form the boundary of a convex body and hence the quantity contains no "pockets" of local minima. This property enables a computer to employ hill-descending techniques in N+1 space which seek a local minimum point. Since, by virtue of the convex nature of the quantity, any point satisfying local minimum conditions must also satisfy absolute minimimum conditions, hill-descending techniques will lead to the required solution.

Several hill-descending techniques for performing a minimization process are being studied and are yielding dependable results. The question of the complete generality of these methods, however, is still an open one.

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[1] Dertouzos, Michael L., "Threshold Element Synthesis", Report ESL-R-200, M.I.T. Project DSR 9891, June, 1964.

E. A LOW-COST TELETYPE-OPERATED GRAPHICAL DISPLAY

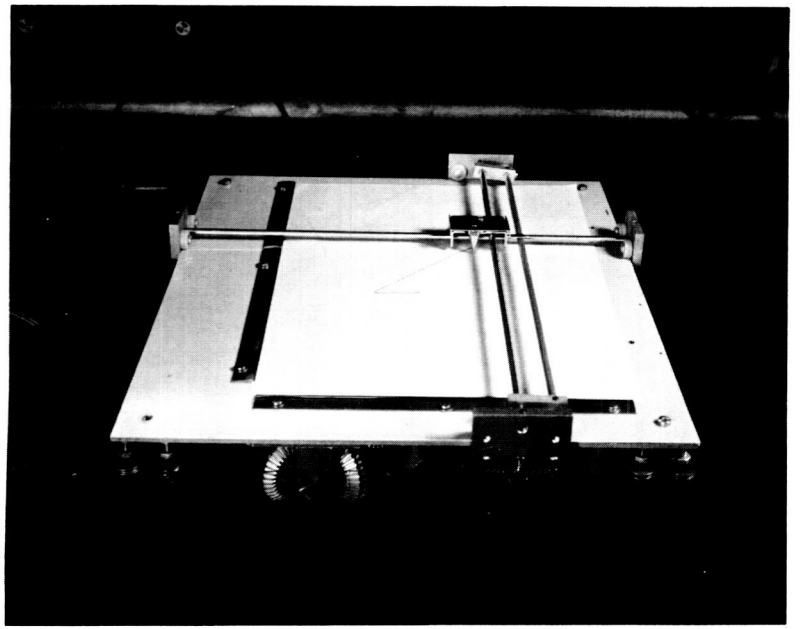
Professor M.L. Dertouzos
Mr. Kenneth J. Olshansky,
Graduate Student

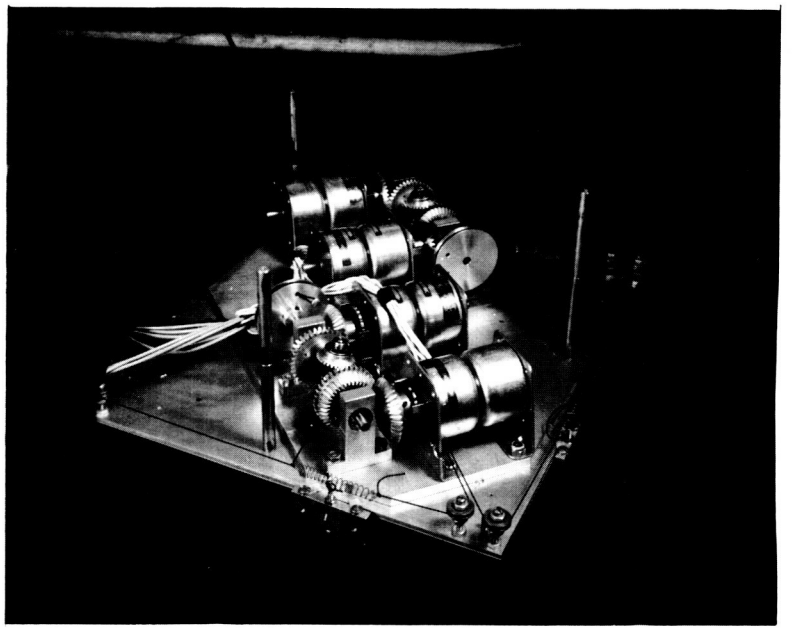
A graphical display device that can be operated from low-speed data sources such as those found in time-shared computer installations is being investigated. The device is basically incremental and produces hard copy. A novel feature of this device is the manner of conversion of binary data into graphical form. This conversion is primarily accomplished by the use of tuned dynamic networks at each axis. Inclusion of mechanical networks, use of certain specific torquers for actuators, and the over-all system organization were motivated by a desire to keep cost at a minimum. This objective does not influence adversely performance or speed of operation. The latter is fundamentally determined by low teletype information rates and by upper bounds on the torque-to-inertia ratios of reasonably-sized actuators. Theoretical extensions of the foregoing basic principle are discussed which will lead to curvature control, data smoothing, high-bandwidth plotting and other desirable properties.

F. SIMULATION OF NONLINEAR CIRCUITS

Dr. Jacob Katzenelson,
Staff Member
Mr. David Evans,
Research Assistant

A general outline of the goals of this research was given in the preceding status report, ESL-SR-225. Presented here is a description of the part of the simulation system which actually calculates the circuit response for any given sources and any initial conditions. The structure of this part, called the analytic part, is described and discussed from two points of view: 1) ability of the system to grow, 2) minimization of computation time. Computer programs implementing the analytic part have been written in AED-0 language[8] and are in various stages of debugging. Once debugged they will enable the system to solve networks consisting of time-dependent sources and RLC elements whose characteristics are piecewise linear and can be either monotonic or nonmonotonic.





A Low-Cost Teletype-Operated Graphical Display

The other parts of the system, which provide the necessary link between the user and the analytic part, are only briefly mentioned here. These parts are in the final planning stage and their implementation will start soon. These parts consist of a data structure which is the representation of the network in the computer and a set of subroutines which perform two functions On the one hand they generate from the data structure all the information required by the analytic part and in the form in which this part needs it. On the other hand, they modify the data structure according to the user's commands. The user's commands are issued through the CADET[9] system which is currently under development by another group in the laboratory. The CADET is a verbal-graphical communication system which accepts commands from the typewriter and the CRT display unit in a form which resembles natural language, interprets them and activates the suitable subroutines.

1. Theoretical Background

This section describes the networks that the system will be able to simulate in its first stage and the method in which this simulation is performed. We are going to follow closely the definitions and the notations of Reference 1, and the reader is referred to that paper for the more technical proofs and procedures.

We assume familiarity with network theory so that the basic concepts need not be defined.[2] A network may be considered as a set of points, called nodes, and a set of connecting branches. Each branch represents a physical two-pole. In this work the branches consist of either a single source or a single element such as a resistor, a capacitor or an inductor. For each of these elements we shall present a simplified definition, narrower than the one given in Reference 1, but sufficient to cover the current work. A two-pole is called a resistor if it is defined, for each time t, by a set of ordered pairs (v, i), where v and i are finite numbers representing all the possible values, at time t, of the voltage and current associated with the resistor. The set of (e, i) is called the characteristic of the resistor and for simplicity it is assumed here that the characteristic is time-invariant. A resistor is current-controlled if, for all currents in the interval

$(-\infty, \infty)$, the voltage e is a (single valued) function of the current i. A voltage-controlled resistor is defined in a dual manner. Figure 1 presents examples of current- and voltage-controlled resistors.

A two-pole is called an inductor if it is defined, for each time t, by a set of ordered pairs (ϕ, i) which represent the instantaneous flux and current associated with the inductor. The voltage across the inductor is given by $e = \frac{d\phi}{dt}$. A two-pole is called a capacitor if it is defined, for each t, by an ordered pair (q, e) representing the instantaneous charge and voltage associated with the capacitor. The current through the capacitor is given by $i = \frac{dq}{dt}$. The flux- and current-controlled inductor, and the charge- and voltage-controlled capacitors are defined as in the case of the resistor.

In this stage of the work we consider only elements whose characteristics can be represented by a function defined on the interval $(-\infty, \infty)$. Thus, resistors represented by Figs. 1a and 1b are acceptable while the resistor represented by Fig. 1c, which is neither voltage- nor current-controlled, will not be considered. An additional condition is imposed in a later section where the characteristics are required to be piecewise linear. (This requirement is imposed in order to gain computation speed and it is not a limitation on the theory or the ability to handle elements whose description by a piecewise linear approximation is not satisfactory.)

Reference 1 discusses in detail the question of existence and uniqueness of the response of networks which consist of the above type of elements and independent sources. It is shown that under certain conditions the response exists, is unique, and is defined by a set of ordinary differential equations satisfying some Lipschitz conditions.[3] These conditions are of two types: (1) the network elements must have characteristics which satisfy suitable Lipschitz conditions; (2) The networks must satisfy certain topological conditions. It should be noted that a network which satisfies (1) and (2) can have elements with nonmonotonic characteristics and that the elements' characteristics need to be continuous but not differentiable.

Let η be a nonlinear RLC network which satisfies (1) and (2) and let us concentrate our attention on the computational aspects of finding the network response.

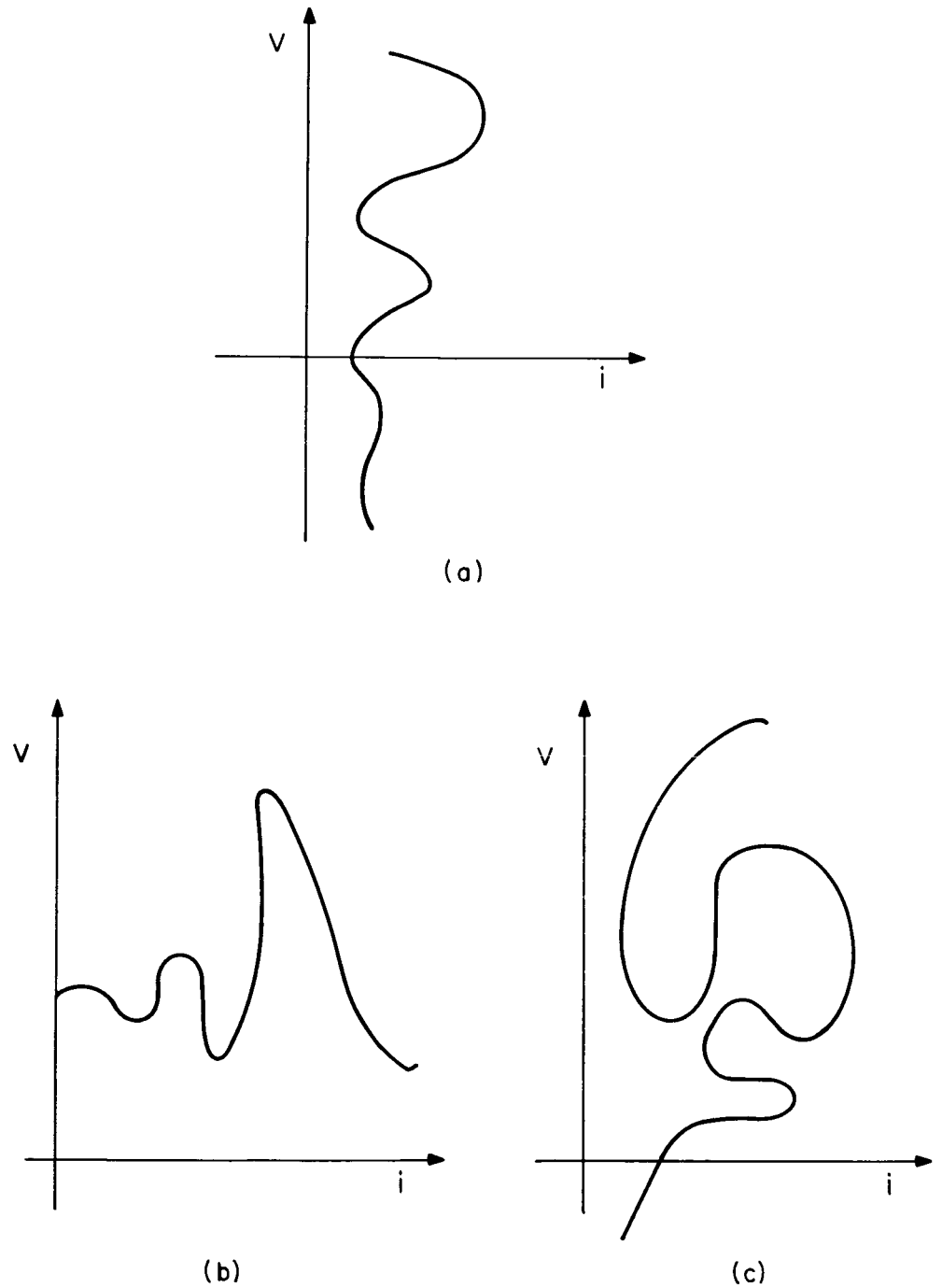


Fig. 1 The characteristics of voltage controlled resistor (a) and current-controlled resistor (b). (c) is neither voltage nor current controlled.

Let us denote the vectors whose components are the voltages and charges of the capacitive branches by $\underline{e}_c$ and $\underline{q}_c$ respectively. Similarly, denote vectors whose components are the voltages and currents of the respective branches by $\underline{e}_r$ and $\underline{L}_r$ respectively; fluxes and currents of the inductive branches by $\underline{\phi}_L$ and $\underline{i}_L$. Voltage and current sources are denoted by the vectors $\underline{E}$ and $\underline{J}$ respectively.

By $(\underline{e}_c, \underline{q}_c)$ we denote the vector whose components are the capacitors' voltages and the capacitors' charges arranged as the notation implies: The capacitor voltages which correspond to $\underline{e}_c$ came first and the capacitor charges, $\underline{q}_c$, second. $(\underline{e}_2, \underline{i}_2)$, $(\underline{\phi}_L, \underline{i}_L)$ and $(\underline{E}, \underline{J})$ are defined similarly.

Assume that initial conditions were applied to the network at time t_o and let us consider the network variable at time t, $t > t_o$. Let us replace each capacitor with a voltage source whose voltage is equal to the voltage of the replaced capacitor and replace each inductor with a current source whose value is equal to the current of the replaced inductor. We are left with a network which contains resistors and sources only. Some of these sources can be eliminated by opening a source from each loop which contains voltage sources only and doing the dual operation on the current source (Section VI of Ref. 1). The resulting network which contains resistors and sources only is denoted by η^R and its sources by $(\underline{E}^R, \underline{J}^R)$.

Now, currents and voltages of η^R are uniquely determined by $(\underline{E}^R, \underline{J}^R)$, and $(\underline{E}^R, \underline{J}^R)$ is a linear combination of $(\underline{e}_c, \underline{E}, \underline{i}_L, \underline{J})$.[1] Let us denote the mapping from $(\underline{E}^R, \underline{J}^R)$ to $(\underline{e}_r, \underline{i}_r)$ by $\underline{f}_R$ and the linear mapping from $(\underline{e}_c, \underline{E})$, $(\underline{i}_L, \underline{J})$ to $(\underline{E}^R, \underline{J}^R)$ by $\underline{\ell}_e^R$ and $\underline{\ell}_J^R$ respectively. We get:

$$(\underline{e}_r, \underline{i}_r) = \underline{f}_R\ (\underline{E}^R, \underline{J}^R) \tag{1}$$

and

$$\underline{E}^R = \underline{\ell}_e^R\ (\underline{e}_c, \underline{E}) \tag{2}$$

$$\underline{J}^R = \underline{\ell}_J^R\ (\underline{i}_L, \underline{J}) \tag{3}$$

Let us now consider the capacitors in the network. Let us replace each resistor and each inductor with a current source with currents equal to the currents of the replaced element. Some of the sources can be

eliminated as the network may now contain cut sets which consist of current sources only. Let us eliminate the extra sources (Section III of Ref. 1) and denote the resulting network by η^C and its sources by $(\underline{E}^C, \underline{J}^C)$. The computation process takes advantage of an analogy between the capacitive network and the resistive network. To establish this analogy we have to define an additional variable. Let τ_c be a tree (or rather a forest as η^C might be unconnected) of η^C. To each fundamental cutset of τ_c we assign a variable q_i equal to the sum of the charges on all capacitors of that cutset. $\underline{q}$ will denote the vector whose components are q_i. The variables $(\underline{e}_c, \underline{q}_c)$ and $(\underline{E}^C, \underline{q})$ of η^C are analogous to the variables $(\underline{e}_r, \underline{i}_r)$ and $(\underline{E}^R, \underline{J}^R)$ of η^R, where $\underline{q}$ plays the role of a "charge source" and, together with $\underline{q}_c$, satisfies Kirchhoff's current law in the same way as $\underline{J}^R$ and $\underline{i}_r$ satisfy it in η^R. Thus we can define the mapping

$$(\underline{e}_c, \underline{q}_c) = \underline{f}_c(\underline{E}^C, \underline{q}) \tag{4}$$

$$\underline{E}^C = \ell_E^C(\underline{E}) \tag{5}$$

where $\underline{f}_c$ and $\underline{f}_R$ both represent mappings from the source space of a one-element-kind network to the space of its branch variables. Since q_i in any fundamental cutset is equal to the sum of the capacitor charges

$$\frac{d}{dt}\underline{q} = \underline{J}^C \tag{6}$$

where

$$\underline{J}^C = \ell_J^C(\underline{i}_r, \underline{i}_L, \underline{J}). \tag{7}$$

Let us consider the inductors in the network. Let us replace each capacitor and resistor in the network by a suitable voltage source, eliminate the extra source and denote the network by η^L and its sources by $(\underline{E}^L, \underline{J}^L)$. As in the capacitive case we choose a forest τ_L of η^L. With each fundamental loop of η_L we associate a variable ϕ_i equal to the sum of fluxes in the loop. Once again we get an analogy between η^L and η^R where $(\underline{\phi}_L, \underline{i}_L), (\underline{\phi}, \underline{J}^L)$ is analogous to $(\underline{e}_r, \underline{i}_r), (\underline{E}^R, \underline{J}^R)$ and $\underline{\phi}$ plays the role of "flux source". Thus we can define the mappings

$$(\underline{\phi}_L, \underline{i}_L) = f_L(\underline{\phi}, \underline{J}^L) \tag{8}$$

$$\underline{J}^L = \ell_J^L(\underline{J}) \tag{9}$$

$$\frac{d}{dt}\underline{\phi} = \underline{E}^L \tag{10}$$

$$\underline{E}^L = \ell_E^L(\underline{e}_c, \underline{e}_r, \underline{E}) \tag{11}$$

We note that $\underline{q}$ and $\underline{\phi}$ play an important role in the circuit. They can be called the state variables and equations (1) through (11) can be reduced to a set of first order differential equations in $\underline{q}$ and $\underline{\phi}$. In addition, for $\underline{E}$ and $\underline{J}$ that are piecewise continuous functions of time, $\underline{q}$ and $\underline{\phi}$ are continuous and differentiable functions of time and therefore they can be evaluated by using standard integration routines.

Figure 2 provides a graphical description of equations (1) through (11). In the next section this figure is discussed in detail with emphasis on the structure of the computation.

2. Computational Structure

Let us consider Fig. 2. Figure 2 describes graphically the relations between the network variables which are expressed in equations (1) through (11). The computational structure of our simulation system corresponds directly to this figure. The blocks of Fig. 2 correspond to "procedure calls." The "input" variables to the call appear on the left, the "output" variables to the call on the right. The arrows indicate transfer of values of variables between the procedures. For example: an arrow from the output of A block to the input of B indicates that the result of A is input for B.

The tall, narrow blocks stand for equations (2), (3), (5), (7), (9) and (11). As was mentioned above, all of them are linear and represent[1] a simple multiplication of the input vector by a suitable submatrix of the (fundamental) cutset matrix. Therefore, these blocks are implemented as two procedures; one of them multiplies a vector by a submatrix and the second multiplies a vector by the transpose of a submatrix.

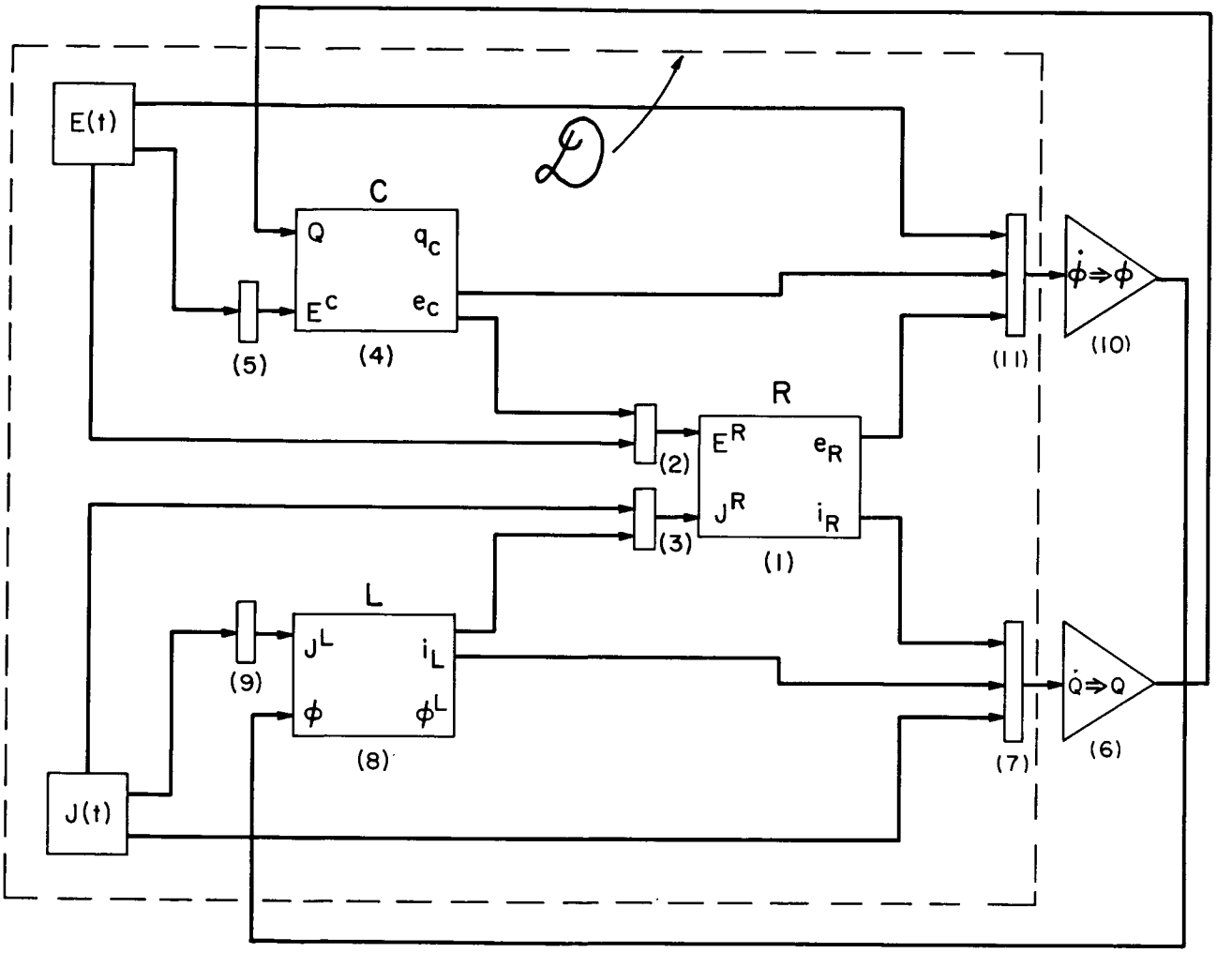


Fig. 2 Computation Structure
(Numbers in parentheses refer to equations in text)

The broken line defines a large block $\underline{D}$ which has an important computational and physical meaning. For each instant of time t, the inputs to this block are the values of the state variables $\underline{\phi}$, $\underline{q}$ and the sources which correspond to time t. The outputs are the corresponding value of $\underline{\dot{q}}$ and $\underline{\dot{\phi}}$. The integration block calls D, and from the values of the state vectors and their derivatives at time t it calculates the values of the state vector for time $t + \Delta t$. We note that the values of the network variables $\underline{e}_c, \underline{q}_c, \underline{e}_r, \underline{i}_r, \underline{\phi}_L, \underline{i}_L$ are evaluated and stored in the process of evaluating the derivatives and these variables constitute the results of the computational process.

As explained above we have built into the simulation system the ability to solve piecewise linear RLC networks. In the following we discuss the ability of the computation structure to be adapted for the solution of network problems which are new or different from those which were programmed into the system. As any new features would remain part of the system, the ability to adapt represents the ability to grow.

As is clear from Fig. 2, the computation structure is partitioned into blocks each performing a certain computation function. Let us consider the integration block: If the user is unsatisfied with the integration formula provided by the system, he can write his own formula and substitute his own procedure to replace the system block of Fig. 2. The type of networks that the system can handle depends mostly on the ability of the block that solves one-element-kind networks. We have programmed into the system a procedure to solve networks whose elements are piecewise linear and for resistors, either voltage or current controlled (charge and voltage controlled for capacitors, flux and current controlled for inductors). By writing a suitable procedure and substituting it instead of the present one, the ability of the system can be extended to handle networks with other types of elements. In particular, this applies to elements whose characteristics are continuous but not piecewise linear (see, however, remarks at the end of Section 3), elements with parametric description,[7] elements with hysteresis, and dependent sources .

The next section contains two topics with a common theme. The topics are (1) the data structure for the variables and its relation to

the procedures, and (2) the procedure for solving one-element-kind networks. The common theme is minimization of computation time.

3. Computation Time, Data Structure of the Variables and the Basic Procedures

The data structure and the procedures which are called to calculate the network response were chosen primarily to minimize computation time. In this section the data structure and the procedures are described, together with consideration of the time element.

From the discussion of the first section it is clear that our main concern is with vector variables. Vectors can most efficiently be handled by storing them as arrays and so enabling the computer to handle them with the help of its index registers. In customary use this approach involves a large waste of space as the size of the array has to correspond to the largest problem the program intends to solve. These conflicting demands of time and space found an elegant solution by using some special features of AED-0.[8] A set of consecutive registers (bead) of the size that the problem demands is first obtained from free storage. Next, a procedure is called in a special way that makes the procedure consider the bead taken from free storage as an array. Once the procedure has returned control to the calling program the set of consequence registers is again considered to be a bead. If it contains results, e.g. values of $\underline{i}_r$ for t - t, it is put on stack and another bead is taken from free storage to accommodate the current values for the nextinstant of time.

As was mentioned in the previous section, the relations expressed in equations (2), (3), (5), (7), (9) and (11) can be expressed as multiplication of a vector by a submatrix (or its transpose) of the fundamental cutset matrix. Matrix multiplication of this nature can be performed extremely fast if the submatrix is formed from consecutive rows and columns of the matrix. This enables efficient use of the computer index registers. This can be achieved by choosing a tree according to Bryant's procedure[1,4] and arranging the elements in the cutset matrix in the way shown in Fig. 3. The network variables are arranged in a single bead which enables the program, when necessary, to handle the currents of the network as one array rather than $\underline{i}_r + \underline{i}_L + \underline{J}$. The

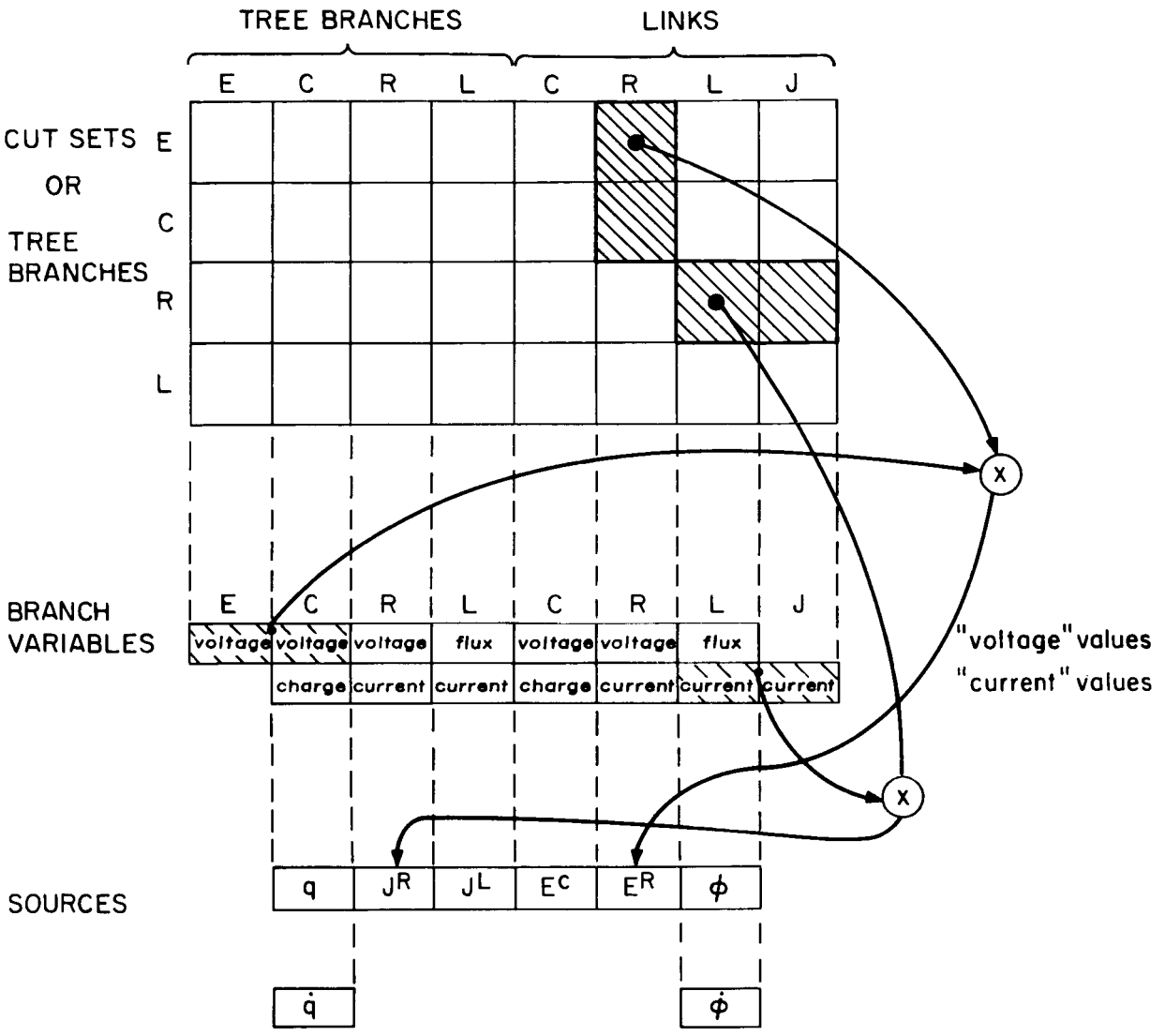


Fig. 3 Arrangement of storage for cut-set matrix and network variables. The arrows and multiplication signs demonstrate the computation of E^R and J^R from $\underline{E}, \underline{e}_c$ and J, J^L.

shaded area is an example of evaluating $\underline{E}^R$ and $\underline{J}^R$ from $(\underline{E}, \underline{e}_c)$ and $(\underline{i}_L, \underline{J})$.

We summarize the discussion of the data structure of the analytic part as follows: The linear array and the matrix are used as the basic data structure (rather than lists of one kind or another) since they provide both an efficient and an elegant computation process.

Let us consider in some detail the procedure which solves the resistive network and calculates the branch currents and voltages $(\underline{e}_r, \underline{i}_r)$ from the values of the sources, $(\underline{E}^R, \underline{J}^R)$. Except in some degenerated cases, this procedure has to solve a set of simultaneous nonlinear algebraic equations, a task which is, relatively speaking, quite time consuming. The necessity for an efficient algorithm to handle this problem can be further stressed if we note that the same operation has to be carried out three times (R, L, C) for each instant of time in which the solution is required.

The procedure uses an algorithm for solving monotonically increasing piecewise linear resistor networks which is described in Reference 5. The advantages are two: 1) The occurrence of linear resistors in the network simplifies the computation considerably. As we expect an electrical network to have a good portion of its resistors linear, this property distinguishes this algorithm from various iteration methods which cannot take advantage of that fact. 2) For time-dependent sources the algorithm computes each solution from the previous one in a rather simple manner which results in a significant reduction of computation time.

A simple explanation of the operation of the algorithm can be given using Fig. 4. Figure 4a presents a simple piecewise linear network. Figure 4b describes the space of the tree voltages where the lines correspond to the loci of the breakpoints. The thick line describes the locus of the solution as the currents are set equal to $k\,\underline{J}_o$ and k is varied from 0 to 1. We call this curve "a solution line". We note that the loci of the breakpoints define regions inside which the network can be described by an equivalent linear network. The algorithm solves these equivalent networks successively as it moves along the solution curve from k = 0 to k = 1. In the first region (A) the inverse of the local conductance matrix of the next region (B) is found by modifying[6]

the matrix of the region (A) rather than by matrix inversion. Thus a difficult matrix inversion is performed only once and all future

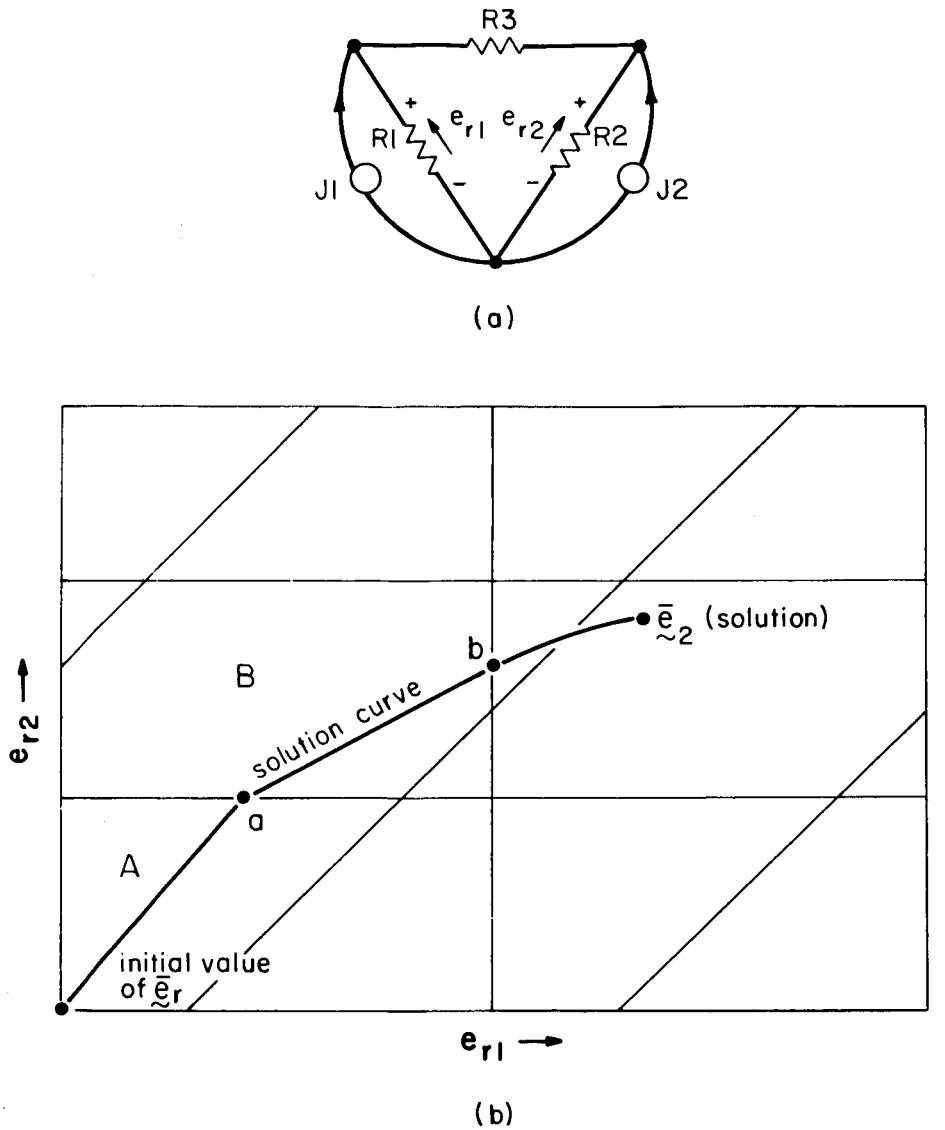


Fig. 4 Solution of a Piecewise Linear Resistor Network

calculations are done by matrix modification with a great saving in time. Experimental runs of this algorithm showed a great reduction of computation time as compared with an iteration method whenever the allowed error which terminates the iteration process defines a small region as compared with a "typical" region defined by the breakpoints.

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9. The CADET System, D. T. Ross and the staff of the Computer-Aided Design group. Unpublished information is available from the authors.

4. Summary and Plans for Future Work

We have discussed in some detail the analytic part of the system for simulation of nonlinear networks. In the discussion and in planning the system we emphasized the minimization of computation time and the ability of the system, once completed, to be adapted to new uses and thus to grow.

The program discussed here has been written and is in various stages of being debugged. Work is in progress on other parts of the simulation system as well. We are near completion of the planning of the part of the system which handles the display of networks on the Electronic Systems Laboratory display console and its associated data structure. By September 1965 we expect to have both parts in operation.

Our immediate future plans are first to complete the system part we are working on now and, second, to incorporate the CADET system as an input device which will enable communication between the user and the program which is more flexible than a simple command system. Other plans include the extension of the system capability along lines discussed in Section 2, mainly to include elements like transistors and tubes.

PART II

CONDUCTION PROCESSES IN THIN FILMS

CONTENTS

A. THERMALLY STIMULATED EMISSION CURRENTS

Professor J.G. Gottling
Mr. W. Stewart Nicol,
Staff Member

A knowledge of the location and energy density of electron trapping levels in thin CdS films is relevant to predicting the behavior of such films when used in space-charge-limited devices. The presence of high-density, shallow-level traps also affects the electronic conduction behavior of the contact region between thin metal films and thin CdS films. The measurement of thermally stimulated emission currents enables the trapping energies and their energy densities to be determined.

The research reported for the previous six-month interval had shown, from Fermi-level analysis, the existence of two electron energy levels at 0.12 eV and 0.37 eV below the conduction band. These were considered to be associated with a shallow donor level and a normal trapping level, respectively. The trapping energy level density was anomalously high, being of the order of 10^{22} per cm^3. The measurement of the variation of dark conductivity, σ_D, with temperature had also shown linear relationships in the $\ln \sigma_D$ vs. $1/T$ curve for several temperature ranges, suggesting the existence of discrete activation energies. Further research was, therefore, necessary during the past six-month interval in order: (a) to verify the predominance of the two energy levels for films deposited under the same controlled evaporation technique as was previously used; (b) to investigate the occurrence of smaller electron populations in other energy levels; (c) to correlate any changes in the energy level structure with changes in evaporation technique, heat treatment, etc.; (d) to evaluate the results of the dark conductivity vs. temperature measurements.

The temperature range over which measurements of current have been made was extended from the range 77°K to 320°K to the range 77°K to 400°K. This was necessary for two reasons. First, it was

believed that a deeper energy level corresponding to a temperature above 320°K could be identified; secondly, the lowest values of dark current at 77°K were obtained by heating the film to approximately 400°K before cooling. It is suggested that this latter process greatly aids the depopulation of trapping levels. The values obtained for the dark current at temperatures above 240°K are extremely important since this is the region where the dark current is converging towards the value of the optically stimulated current.

The results of the past six-month interval show that the two thermally stimulated current peaks again appear for all diodes, one in the vicinity of 90°K and one between 280°K and 340°K. The trapping energy levels calculated by the method of Bube,[1] corresponding to these peaks, lie between 0.12 eV and 0.14 eV, and between 0.37 eV and 0.42 eV. The trapping energy density for the more deeply lying level is still of the order of 10^{22} per cm^3 for all diodes measured.

As was stated in the previous report, this anomalously high value should be reduced in proportion to the photoconductive gain, if the large thermally stimulated current is the result of electrons circulating through the film more than once before suffering recombination. An alternative explanation that removal of holes produces a negative space charge in the vicinity of the blocking contact, thereby effectively reducing the barrier height and increasing the thermally stimulated current, is also possible.

Energy levels having correspondingly smaller thermally stimulated peak currents have been found at 0.31 eV, 0.33 eV, and 0.34 eV, in the vicinity of the dominant energy level.

An attempt has been made to correlate treatment of the surface of the CdS film, before deposition of the blocking electrode, with the trapping energy level structure. A technique was introduced of evaporating a layer of sulfur (< 100 Å thick) directly onto the CdS film surface at room temperature. The film temperature was then raised to 90°C over a period of 3 minutes and cooled to room temperature before deposition of the blocking electrode. No further heat treatment was found to be necessary to produce diodes having reverse

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[1] Bube, R.H., Photoconductivity of Solids, p. 294, Wiley.

breakdown voltages between 8 and 9 volts. Energy levels of 0.14 eV, 0.36 eV and 0.47 eV were obtained for diodes of this category. The 90°K peak corresponding to 0.14 eV is especially pronounced. This result is consistent with that of Kulp and Kelley[2] who find that interstitial sulfur contributes to an edge emission center 0.14 eV below the conduction band. Since these diodes have much smaller dark currents, the conductivity increases very steeply in approaching this temperature.

From measurements of the variation of the dark current, i_D, with temperature, electron activation energies, E_a, were obtained for temperature ranges where the current variation of the form $i_D = i_{OD} \exp(E_a/kT)$ was observed to hold. For films which had only argon ion bombardment of the CdS surface before evaporation of the gold blocking electrode, values of E_a are 0.01 eV, 0.034 eV, 0.043 eV for temperatures below 170°K and 0.04 eV, 0.33 eV and 0.59 eV for temperature above 170°K. The value 0.33 eV was found for all films. For films which had an evaporated sulfur layer, much lower activation energies were found: typically 0.004 eV, 0.12 eV and 0.29 eV for the highest range of temperature. The reproducibility of activation energies for one film having only argon ion bombardment was shown by cycling the film over the range of dark current measurements five times during a period of several days. For each cycle the current at 77°K was different. In all cycles E_a values of 0.06 eV and 0.33 eV appeared, although the currents at 77°K differed by one or two orders of magnitude. These differences in current are considered as being due to differences in occupancy of the trapping levels.

The spatial location of trapping centers is not yet known. As previously mentioned, high-density, shallow trapping levels in the vicinity of a metal--semi-insulating film contact affect the conduction properties of the contact. It will, therefore, be of advantage to measure any changes in the energy location of the trapping levels which result from CdS film surface treatments.

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[2] Kulp, B. A., and Kelley, R. H., J. Appl. Phys., 31, 1057 (1960).

B. MEASUREMENTS OF BARRIER HEIGHT, BARRIER WIDTH, AND IMMOBILE ION DENSITY

Mr. W. Stewart Nicol,
Staff Member

The band structure in the vicinity of the thin metal--CdS film contact determines the linear or nonlinear behavior of the contact. Measurements of barrier height, V_D, barrier width, t_o, and immobile ion density, N_D, in the vicinity of the blocking contact can be conveniently made by finding the variation of the junction incremental capacitance with applied bias voltage.

During the past six-month interval a series of measurements of V_D, t_o, and N_D has been carried out on three categories of diode junctions. The diodes investigated were Au-CdS-Au diodes whose blocking contacts were formed, in all cases, in the region of the gold electrode evaporated over the CdS. The gold electrode evaporated directly onto the substrate before the CdS evaporation always behaved as an injecting electrode. The three categories are related to the contact-formation process as follows:

Category I: The injecting electrode and CdS film are evaporated. The CdS surface may then be treated by argon ion bombardment prior to the evaporation of the second electrode. The ion bombardment is sustained for two minutes at 2 KV and 50 microns pressure, and is carried out when the film is at room temperature. Following the evaporation of the second electrode, the complete diode structure is annealed at 300°C for several minutes in air at atmospheric pressure. It has been verified that argon ion bombardment is not essential to the formation of this class of diode, but that for most diodes it has enhanced the formation process.

Category II: The injecting electrode and CdS film are evaporated, followed by annealing at 10^{-5} mm pressure. Annealing times and temperatures range from 1/2 hour at 360°C to 1 hour at 320°C. The film is then cooled to room temperature and the surface may be subjected to argon ion bombardment as for Category I. Again, it has been verified that argon ion bombardment is not an essential part of the formation process, but does enhance it. The second electrode (- 200 to 400 Å gold) is then evaporated after the annealing.

Category III: The injecting electrode and CdS film are evaporated, cooled to room temperature, and an artificial blocking layer of less than 100 Å sulfur is evaporated in 10^{-5} mm pressure. Following the evaporation the substrate is heated to 90°C over a period of 3 to 5 minutes, then cooled to room temperature and the second electrode evaporated.

The value for V_D was obtained by extrapolating the linear relationship of $1/C^2$ vs V_a, in which C is the incremental capacitance, C_o, for zero applied bias voltage, using $t_o = \epsilon A/C_o$. The immobile carrier density, N_D, was found from the slope of the linear region of the curve $1/C^2$ vs V_a and the theoretical relationship

$$N_D = \frac{-2}{qA^2\epsilon}\left\{\frac{d(1/C^2)}{dV_a}\right\}^{-1}$$

All capacitance measurements were made at 1 Kc/s

1. Measurements of V_D, t_o, and N_D at Room Temperature

For diodes in Category I, the variation of $1/C^2$ with small bias values is extremely rapid, leading to very low barrier heights. For these diodes the linear part of the curve extends only over a 100 mV range. For diodes in Categories II and III the linear region extends over a 1-volt range, with a less rapid variation in $1/C^2$. The following table gives values for V_D (uncorrected for the presence of an insulating layer), t_o and N_D

Diode Category	Barrier Height V_D Volts	Barrier Width t_o Angstroms	Immobile Ion Density N_D per cc
I	0.02	430	10^{16}
II	0.90	290	10^{18}
III	1.63	630	5×10^{17}

The correction[3] for the possible existence of an insulating layer at the surface cannot be applied since the thickness is not known exactly

[3] Goodman, A. M., J. Appl. Phys., 34, 335, (1963)

For the sulfur diode an upper bound on the thickness is 100 Å, estimated from the amount evaporated. However, the correction is then unrealistically large. Therefore, only a fraction of the evaporated sulfur forms on the surface. In the case of $V_D = 0.02$ volt, further measurements have to be taken to verify whether or not it is anomalous.

2. Behavior of Barrier Height, Barrier Width, and Immobile Ion Density at 77°K

The measurement of V_D, t_o and N_D at 77°K has been made for a Category II diode. Before capacitance readings were taken, the diode was stored in darkness for several hours. Applying a reverse bias voltage increased the zero-bias capacitance C_o. With repeated excursions of the reverse bias to the maximum value used, the value of C_o at first increased with each excursion and finally reached a steady value. At this stage a repeatable variation of incremental capacitance with both reverse and forward bias could be obtained. The following table summarizes the results.

Diode Category	Barrier Height V_D Volts	Barrier Width t_o Angstroms	Immobile Ion Density N_D per cc
II	1.56	1000	2×10^{17}

The incremental capacitance for zero bias voltage was found to be an increasing, linear function of temperature.

Further measurements in this area are necessary: (a) to study the effects of a much wider range of surface treatments; (b) to investigate the low values for V_D for diodes in Category I; (c) to obtain information about surface states through capacitance measurements at various frequencies.

C. OPTICALLY MODULATED CONDUCTIVITY WITH VOLTAGE DE-EXCITATION

Professor J.G. Gottling
Mr. W. Stewart Nicol,
Staff Member
Mr. Hans Jenssen,
Undergraduate Student

Research conducted during the previous six-month interval had shown experimentally that the conductivity of thin CdS films could be increased by an order of magnitude with optical stimulation and then restored, or "de-excited", to its original value by the application of voltage pulses. The influence of electric fields on photoconductivity has been reported for single crystals of CdS,[4, 5, 6] whereas this research was conducted for polycrystalline evaporated CdS films. The interpretation of the effect of high electric fields on single crystals is different for different authors. Boer and Kummel suggest that high electric fields free electrons from traps. Kallmann and Mark interpret their data as a decrease in the probability for retrapping. Bube indicates that this could be the result of space-charge-limited currents injected by high fields. Their data are taken from decay curves with the high fields applied for a period of time of from one to several minutes. Further research on conductivity modulation of thin CdS films was, therefore, necessary during the past six-month interval in order: (a) to investigate how large a change in conductivity can be obtained with voltage pulses; (b) to obtain the relationship between percentage change in conductivity and amplitude and duration of voltage pulse--possible storage device applications of the phenomenon require that the effect of short de-excitation pulses be found; (c) to identify which effect is mainly responsible for voltage de-excitation in thin films.

This recent research period has shown that the photoconductive decay for all CdS films investigated was confirmed as obeying the

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[4] Kallmann, H., Mark, P., Phys. Rev., 105, 1445, (1957).

[5] Boer, K.W., Kummel, U., Ann. d. Physik, 6, 303, (1957).

[6] Bube, R.H., Photoconductivity of Solids, p. 292.

relation $i \sim t^{-a}$ after a rapid (less than 1 second) initial decay. This is consistent with the presence of trapping energy levels. It was found that voltage pulses shorter than 100 microseconds had little effect on the decay of conductivity, and this was quite independent of pulse height. For pulses longer than 100 microseconds, the percentage change in conductivity is proportional to the logarithm of the pulse length. When the pulse length was 100 milliseconds, "saturation" of the percentage change of conducitivity was reached; longer pulses did not change the conductivity further. Pulses in the reverse-bias direction were more effective than forward-bias pulses.

It was concluded that the mechanism for voltage de-excitation was an increase in the probability for recombination or a decrease in the probability for retrapping and is an effect of injected carriers rather than field excitation from trapping levels. This is in agreement with the results of Kallman and Mark.[4] Further details of results obtained in this research are given in the following thesis:

"De-Excitation of CdS Films by High Electric Fields", Hans P. Jenssen, S.B. Thesis, M.I.T., (June, 1965).

D. GRID-STRUCTURE FORMATION OF METAL FILMS

Mr. Anthony A. Aponick, Jr.,
Research Assistant

The study of metal-film structure as determined by applied voltage and substrate temperature has been concluded. In this work we found that metal-film grids on CdS can be formed to dimensions suitable for use as grids in thin-film solid-state triodes. The results of this work appear in Technical Report ESL-R-237, "An Investigation of Thin-Film Gold Structures on CdS", by A. Aponick. The abstract of this report is reproduced below:

"Previous electron microscopic investigations of the structures of gold thin-films deposited on CdS surfaces have shown that these structures can be made electrically discontinuous with thermal treatments. This phenomenon is shown to exist for gold surface mass densities up to 30 $\mu g/cm^2$.

An investigation is made of the possibility that high electrostatic fields can be used to exert sufficient force on the discontinuous gold grains during annealing to cause the

formation of "bridges" between them. It is shown that this procedure is not useful for the formation of grid-like structures.

A theoretical treatment is presented which shows that annealing phenomena can be explained with an atomic gold gas model. The theory predicts that "solid-layer" structures are not stable at high substrate temperatures.

A means of fabricating grid-like sturctures with 40-50 per cent open area and sheet resistance of 12-50 ohms per square is described in detail. The method of production is found to be a consequence of the gas-model."

E. TRIODE CONSTRUCTION AND FORMATION OF BLOCKING AND GRID CONTACT

Mr. Anthony A. Aponick, Jr.,
Research Assistant

Prior work by our group has established a procedure for obtaining thin-film metal grids which possess suitable aperture dimensions ($\cong$2000 Å across the shortest distance of the aperture) for device work. Therefore, it is reasonable to turn to the task of constructing a triode.

From our work with CdS as an insulating film and Au or Ag as a metal grid, we can anticipate the following steps for the fabrication of a triode:

a. A 300 Å metal cathode film is deposited onto a glass substrate at room temperature.

b. A 2000-6000 Å CdS film is deposited over the cathode with the substrate at 100°C. The deposition proceeds for one hour; and the CdS insulation surface is Type IV, as described in Report ESL-R-229.

c. An oxygen glow discharge is applied to the surface for 30 minutes at a pressure of 100 microns Hg. The substrate temperature is 180°C.

d. The substrate is heated to 400°C for one hour to form a layer of near-intrinsic CdS at the surface due to diffusion of oxygen.

The above steps provide a substrate for the grid film, which leads to a blocking contact between the grid and the CdS. This procedure is essentially the same whether the grid is to be made of Ag or Au. Following step (d) the dielectric triode is completed by:

e. Deposition of a metal grid film
f. Formation of grid apertures by heat treatment
g. Deposition of CdS onto the metal grid
h. Deposition of a metal anode film

The principal difficulty, which must be overcome in order to obtain a dielectric triode with useful current-voltage characteristics, is to achieve a blocking contact between the metal grid film and the overlying CdS film. The necessary blocking contact between the grid film and the CdS film underneath it, has been obtained. Two possible mechanisms can account for the formation of this blocking contact:

1. Metals such as Ag or Au have a natural tendency to form a blocking contact on CdS, because they behave as an impurity acceptor within the CdS. Consequently, if some of the grid atoms penetrate into the CdS they reduce the effective density of donors present on account of sulfur deficiencies. The CdS surface is then converted into more intrinsic material. This process apparently is facilitated by deposition of the grid film onto the underlying CdS.

2. Oxygen, a residual component of the vacuum, can enter substitutionally into the CdS structure replacing sulfur deficiencies. This process produces more intrinsic material at the surface of the insulator. The occurrence of the oxygen block can be enhanced by exposing the CdS surface to an oxygen glow discharge before deposition of the metal grid.

Both of these forming processes are effective on underlying CdS. However, the formation of a satisfactory blocking contact between the grid and an overlying CdS film remains to be accomplished. The following approaches to the solution of this problem are in progress:

a. Sulfide formation on the grid through exposure to H_2S

b. Oxidation of grid surface by a heat treatment in oxygen or an oxygen glow discharge

c. Deposition of a sulfur layer by evaporation

d. Use of a p-type silicon grid with SiO_2 isolation.

F. FRINGE-STEP MEASUREMENTS

Professor J. G. Gottling
Mr. W. Stewart Nicol,
Staff Member

During routine film thickness measurements of CdS during the last six-month period, we observed a step-like structure of the optical interference fringes at the edges of the CdS films, where the thickness gradually tapers off to zero due to shadowing of the substrate by an evaporation mask. If this structure is a linear image of the film thickness profile, then these observations can imply that CdS films consist of crystalline layers. At the boundary of each layer a blocking contact is expected to occur. This situation is undesirable for device-quality films, because each blocking contact adds unmodulated series voltage drop to the external terminal characteristics of the device.

We have investigated this fringe structure phenomenon in order to determine if it is related to a structural characteristic of our films or is simply a natural optical phenomenon. A number of CdS films with various values of thickness were deposited and these were observed with various wavelengths of monochromatic light. The current-voltage characteristics of Au-CdS-Au diodes formed using these CdS films were measured. In the forward direction (positive voltage applied to the top Au electrode) the current was found to vary as

$$I = I_o \exp \{qV/akT\}$$

where I_o is a constant, q is the electronic charge, V is the applied voltage, k is Boltzmann's constant, T is the temperature, and a is a constant as determined from the slope of a plot of ln I vs. V. If crystalline layers exist in the CdS film and these provide identical blocking contacts, then the applied voltage V would be distributed

equally across each barrier. The current-voltage characteristic of a diode formed with such material is then expected to have the above form, where the constant a correlates with the number of crystalline barriers. However, the number of steps observed at the edges of the films did not correlate with the value of the constant a.

As a result of this work, we have established that the fringe steps are related to a natural optical interference phenomenon which occurs in double-layer films. Fresnel reflection-coefficient analysis of the double-layer interference has been used to determine the relationship between fringe displacement and film thickness. The result of the analysis is a nonlinear relationship which predicts that the interference fringes displace in a step-like manner if the film thickness changes smoothly. The analysis provides a convenient thickness measurement procedure for transparent films which does not require an overlay contour film that might interfere with subsequent use of the transparent film. This work is now completed, and a description of the observations and theory will be included in a report currently being prepared.

G. NEGATIVE RESISTANCE OF CdS FILMS

Professor J.G. Gottling
Mr. W. Stewart Nicol,
Staff Member
Mr. Michael Oliver,
Undergraduate Student

A current-controlled negative resistance (CCNR) has been observed by our group in CdS films.[8,9,10,11] Because the performance of the dielectric triode is determined by the conductivity behavior of the CdS insulator film, it is important to understand

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[8] Geppert, D.V., Proc. I.E.E.E., 51, 223, (1963).

[9] Chopra, K.L., J. Appl. Phys., 36, 184, (1965).

[10] Beam, W.R., Armstrong, A.L., Proc. I.E.E.E., 52, 300 (1964).

[11] Litton, C.W., and Reynolds, D.C., Phys. Rev., 133, A536 (1964).

the mechanism responsible for this phenomenon. Experimental work has been conducted toward this objective.

The characteristic features of the negative resistance in CdS are:

a. The phenomenon is a current-controlled volt-ampere characteristic which occurs primarily with the blocking contact at a positive potential.

b. Voltage peak-to-valley ratio is not pronounced and ranges from about 1.1 to 1.6 for our observations.

c. No pronounced temperature dependence for operation near room temperature.

d. Transient phenomena occur for transition into and out of the highly conducting condition.

e. Localized damage occurs after prolonged operation in the negative-resistance region.

Various theories have been proposed to account for this negative-resistance phenomenon. Chopra[9] has proposed that an avalanche mechanism similar to gaseous breakdown is responsible. Beam and Armstrong[10] suggest that an ionic forming process occurs in a thin (25 Å) insulating region adjacent to the electrode, converting this region into a semiconductor. Lampert[12] has considered the situation where two-carrier injection occurs, and he shows that the onset of double injection produces a negative resistance. Litton and Reynolds[11] believe that double injection accounts for their observation of negative resistance in CdS "tap" crystals at low temperatures.

The ion-drift mechanism appears to be an unlikely explanation for our observations, since the effect is relatively insensitive to temperature. Conditions in the CdS diode are not favorable for hole injection from the anode, since the barrier for hole injection is probably about 1.8 eV. Also, the field is probably distributed uniformly across the full diode width so that at the voltage peak the field is about 5×10^4 volt/cm. Therefore, tunnel injection of holes is not likely. The avalanche mechanism appears to be a more reasonable explanation for this effect.

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[12] Lampert, M. A., Phys. Rev., 125, 126, (1962).

H. P-TYPE CdS FILMS

Professor J.G. Gottling
Mr. Walter Gajda, Jr.,
Graduate Student

P-type single crystals of CdS have been prepared in bulk samples[13, 14] by sublimation of copper doped CdS powder and by evaporation of Cu onto CdS with subsequent diffusion. An attempt has been made through a Graduate Student thesis project to form p-type CdS films by diffusion of Cu throughout the film. The availability of p-type CdS is of interest because it will permit greater versatility in device fabrication. The abstract of Mr. Gajda's thesis is given below; the thesis is available at the M.I.T. Library.

> "The effects of the addition of copper to thin films of CdS were investigated by a number of techniques.
>
> It was concluded that p-type CdS can be produced by an amount of copper in the range of 1.5 - 5.0 per cent by weight. Above 5 per cent the copper asserts itself strongly in the CdS lattice and n-type conduction results. Below 1.5 per cent the normal n-type tendency of evaporated CdS is dominant.
>
> The Seebeck Effect was used as a primary means of determining carrier type. Measured Seebeck coefficients were extremely low, on the order of 1 $\mu V/^{o}C$. Experimental difficulties precluded the use of the Hall Effect; extremely low mobility is postulated as the reason for the problem involving Hall Effect measurements.
>
> P-N diodes were also successfully fabricated. However, reverse characteristics proved to be extremely leaky. Capacitance was inversely proportional to the one-half power of the reverse bias, as expected for an abrupt junction.
>
> Detailed information concerning the diffusion kinetics of copper into CdS was gathered and two hypotheses explaining the p-type doping effect of copper were also proposed."

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[13] Reynolds, Greene, Wheeler, and Hogan, Bull. Am. Phys. Soc., 1, 111, (1956).

[14] Woods, J. and Champion, J.A., J. Elect. and Control, 7, 243 (1959).

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